IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of		PATENT APPLICATION
Inventor:	Yoshi Ono, John F. Conley, Jr., and Pooran Chandra Joshi	June 17, 2005
Serial No.:	10/805,158	ATTORNEY DOCKET No. SLA0830
Filed:	March 19, 2004	Group Art Unit: 2814
Title:	CHARGE TRAP NON-VOLATILE MEMORY STRUCTURE FOR 2 BITS PER TRANSISTOR	Examiner: Marcos D. Pizarro-Crespo
		Confirmation No. 8642

CERTIFICATE OF TRANSMITTAL UNDER 37 C.F.R. § 1.8

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David C. Ripma, Reg. No. 27,672
Date : June 17, 2005

RESPONSE TO RESTRICTION REQUIREMENT

Mail Stop Non-Fee Amendment
Hon. Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This communication responds to an Office Action dated

May 18, 2005 in the above-identified patent application. In the Office Action the Examiner requires restriction to one of the following inventions:

Group I. Claims 1-15, drawn to a device; and

Group II. Claims 16-26, drawn to a method.

Applicants elect to pursue the Group II claims, claims 16-26, drawn to a method.

Respectfully submitted,

Date: 6/17/05

By: _____
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